Porting of a spectropolarimeter on Digital Base Band Converter

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Abstract

The Digital Base Band Converter (DBBC) is a hardware platform based on programmable logic, developed by IRA-Noto, being installed on all antennas of the EVN network. SRT will also be part of this network and therefore it will be equipped with this system for VLBI observations; as these observations will be performed during two months every year, one can take advantage of DBBC's reconfigurability to use it also during single dish observations.

In this paper we describe the porting on DBBC of a spectropolarimeter developed at Arcetri Astrophysical Observatory for a multi-feed receiver for Sardinia Radio Telescope. We will first describe the overall system and then all design modifications required to make the device compatible with the new hardware.

1 Introduction

The Digital Base Band Converter [1] is a hardware platform, developed at IRA-Noto, which is based on programmable logic. The main idea of the DBBC project is to replace the existing, obsolete VLBI terminal with a complete and compact system that can be used with any system for recording and storing radio astronomical data. The entire project is based on a flexible architecture, consisting of one or more FPGA boards as computing elements. Figure 1 shows a block diagram of the system:

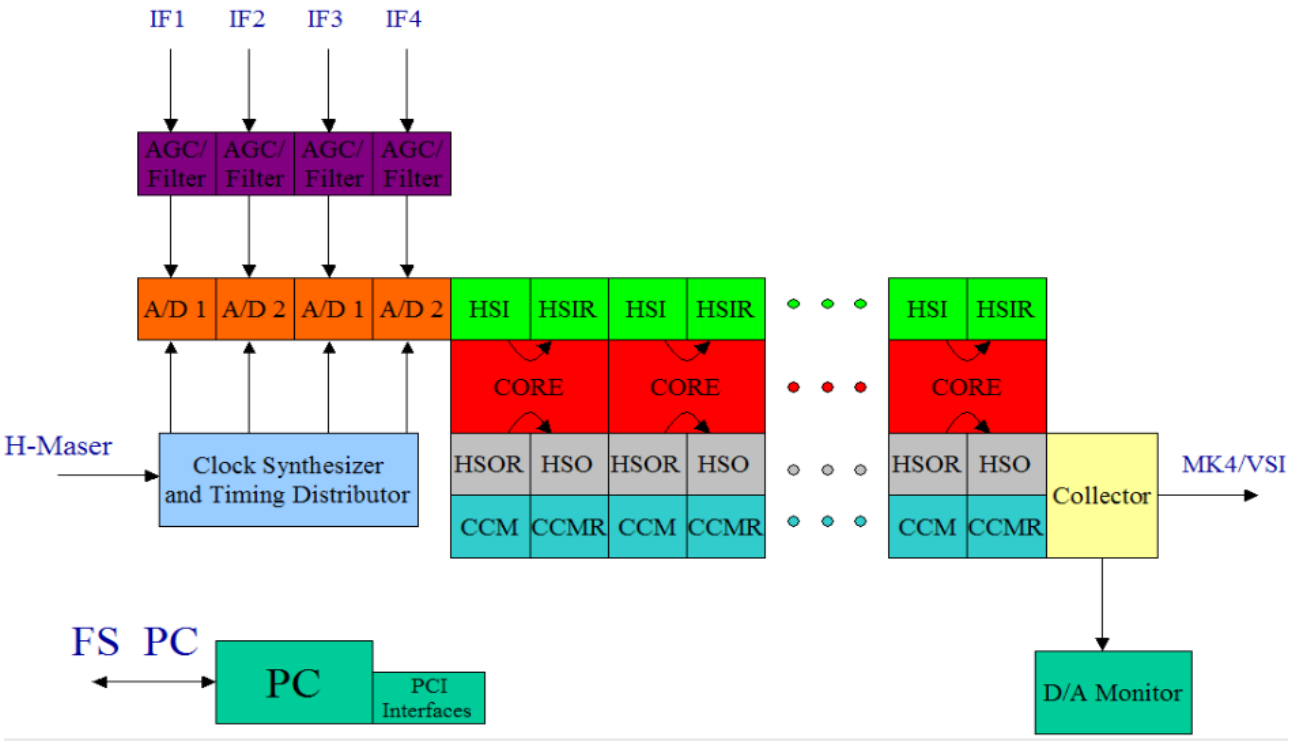

Figure 1: Block diagram of DBBC

The intermediate frequency signals goes through the anti-aliasing filter and then through the analog-to-digital converters. Once the data are in digital format they are sent to the high-speed bus (HSI, HSO, CCM) connected to the various boards with Xilinx FPGAs Virtex5 within which the signals are processed.

The system also includes a computer control and hardware to manage the clock and a board for digital-to-analog conversion.

This platform, designed and engineered for VLBI observations, has been examined in details by the electronics group of the Arcetri Observatory in order to use it for other applications, using the

reconfigurability of the FPGA boards. One such application is a multi-channel spectropolarimeter which was designed as a back-end for a multi-feed receiver for the Sardinia Radio Telescope (SRT).
After a brief description of the system, we discuss the work on porting the spectropolarimeter on DBBC, and then we describe all the design steps performed to adapt the original code to the new system.

2 Spectropolarimeter for the multi-feed receiver

In this work we ported on the DBBC the design for an existing multi-channel spectropolarimeter, that has been built as a back-end for a multi-feed receiver developed for the SRT.
Figure 2 shows a picture of the multi-feed receiver, consisting of seven adjacent feeds, with a bandwidth in the range 18-26 Ghz, and capable of separating right- and left-handed circular polarization. This receiver requires a multi-channel back-end, to simultaneously analyze the signals from the seven feeds.

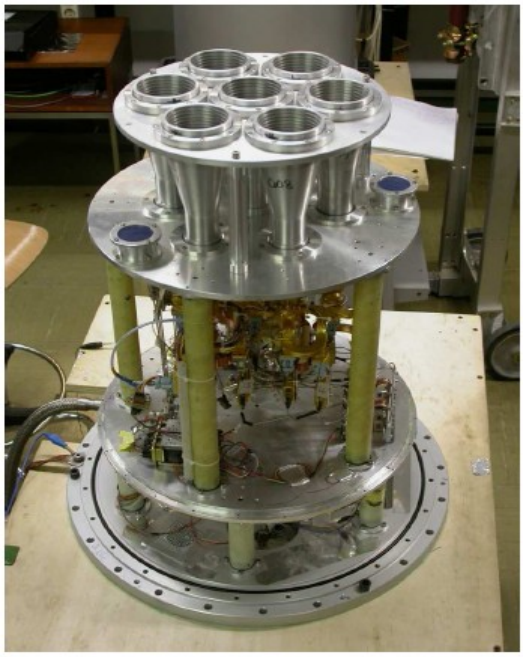

Figura 2: Multi-feed receiver for SRT

The specifications for the back-end of the multi-feed receiver are the following:

- A total of 14 channels, corresponding to seven dual-polarization pairs;
- High flexibility, sensitivity and stability;
- Total instantaneous bandwidth of at least 80 MHz;
- Ability to restrict the bandwidth down to 0.5 MHz;
- High resolution, corresponding to 4096 spectral channels;

This multi-channel spectropolarimeter ([2], [3]) can process simultaneously fourteen signals, at the intermediate frequency, at the output of the receiver.

The system is built on four circuit boards, two sampler and two processing boards respectively, built employing Altera and Xilinx FPGA devices. In Figure 3 we show these boards:

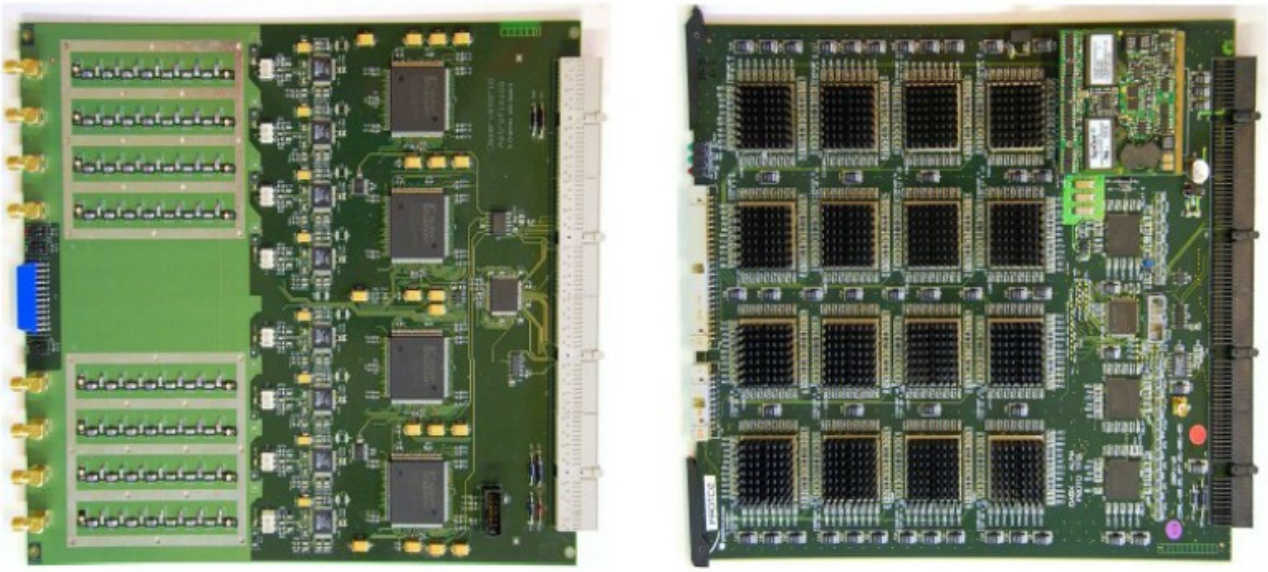

Figure 3 :Boards used to make the back end. Left: ADC board, right: FFT board

In figure 4 we show a block diagram of the back-end, relative to 8 channels:

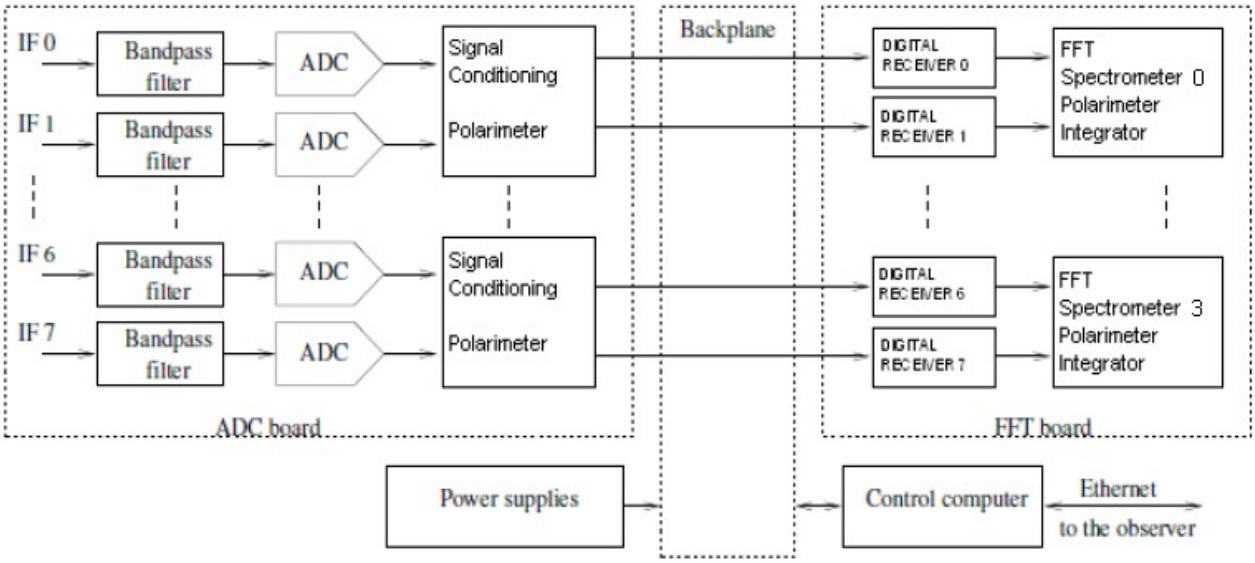

Figure 4: Block diagram of the back-end

The functional blocks shown in figure 4 perform the following functions

Band pass filters: They perform a reduction in bandwidth of the polarized signals at intermediate frequency. The -3 dB effective bandwidth of each filter extends from 140 to 220 MHz. This device is designed to provide a high rejection outside the bandwidth in order to avoid aliasing.

ADC, Analog to Digital Converter: The two orthogonally polarized signals are sampled individually with two equal ADC having a resolution of 8 bits and a sampling frequency of 250 MHz. The ADC has a conversion window of +/- 0.5 V divided in 256 equal channels, (4 mV step). The ADC operates in its second Nyquist window, down-converting the input signal to base-band, between 0 and 125 MHz.

Signal Conditioning: To maximize the performances of the spectrometer the data flow of real-valued samples at a frequency of 250 Msample/s is converted into complex-valued samples at a frequency of 125 Msample/s.

Broadband polarimeter: This module performs the calculation of the four terms defining the Stokes parameters and integrate them for a user-programmable time. The estimation of the Stokes parameters is performed using the spectral density integrated over the entire bandwidth of the analog filter.

Digital receiver: Depending on the required radio frequency and spectral resolution, it is important to vary the width of the band being analyzed. The signals from the first board are processed separately by two digital receivers, each with a local oscillator and a filter that reduces the bandwidth and sampling rate. The instrument provides nine values of decimation, corresponding to a maximum bandwidth equal to the input bandwidth (125 MHz) and a minimum of 0.5 MHz. For polarimetric measurements it is important not to introduce phase shifts between the two polarimetric channels that will be combined together. To avoid this effect, the two local oscillators are programmed simultaneously so that both have the same initial phase.

FFT (Fast Fourier Transform) spectrometer : This is equivalent to a bank of band-pass filters that process the same analog signal and reconstruct adjacent portions of the spectrum. Each filter provides a spectral channel with the same bandwidth and uniformly spaced in the input bandwidth. The spectral response of each channel must provide isolation between adjacent spectral channels.
The FFT algorithm is an efficient way to calculate estimates of the power spectrum. The number of spectral points is fixed by design and is limited by the available memory on the FPGA. A sequence of N-time samples are converted into N complex spectral channels in real-time.
This module can produce simultaneous spectra from two independent signals. This is possible because the spectrum of a single signal is calculated in N/2 clock cycles. The operations of the FFT is performed at a clock speed corresponding to the decimation factor set in the filter of the digital receiver shown in Fig.4, therefore the duration of a FFT cycle increases with decreasing bandwidth.

Polarimeter: computes the auto- and cross-correlation of the two polarization signals, allowing the calculation of the Stokes parameters.

Integrator: the four parallel output signals from the polarimeter are integrated for a programmable time, up to several seconds. The integration scheme uses a dual memory: the first one integrates the signal for a pre-set time while the other memory is read by the control PC. The integration time is set externally as an integer number of FFT cycles.

3 Porting of the spectropolarimeter on DBBC

As described in the previous chapter, the system design includes four boards for a total of 40 FPGAs of which 8 are Xilinx FPGA and 32 are Altera FPGA. The current DBBC under test consists of a single Xilinx FPGA Virtex5 LX220. We have also modified the code to perform porting to the new platform, taking into consideration the different hardware for converting the analog/digital signal acquired, as we describe in the next sections.

3.1 Analog-to-Digital conversion of the signal acquired

The DBBC has a digital board for signal acquisition with an analog-to-digital converter operating at 1.024 GHz. As previously described, the input digital signals arrive at the spectropolarimeter with a rate of 250 MHz (which in our case becomes 256 MHz since the DBBC use a clock of 128 MHz instead of 125), therefore we have to make a decimation of a quarter of the input samples. However, in the ADC board the first operation is to "split" the 250 MHz flow in two 125 MHz streams using "Double Data Rate" functions, then the signals are processed in two parallel streams, each with a reduced rate of 125 MHz. After the conversion from real to complex format, these data streams represent the real and imaginary part of the original signal at 250 MHz.
The DBBC also uses a system of "Double Data Rate": the fast rate (1.024 GHz) of the input signal is converted into 8 lower-rate (128 MHz) “parallel” signals, thus eliminating the older "Double Data Rate" functions. The new inputs for the "Signal Conditioning" stage are represented by the first and fifth signal of the new “parallelized” output.

3.2 Verilog-VHDL translation

To program the FPGA we must use hardware description languages, such as Verilog and VHDL, originally developed for different purposes. Even if the two languages are essentially equivalent, we avoid using them in the same system, because some synthesis tools do not always properly synthesize codes written with different languages.
The original system was written largely in VHDL but some parts have been developed in Verilog, and in particular the module that performs the integrations of the spectra. These modules have now been converted

into VHDL.

3.3 VHDL coding of modules generated by proprietary tools

As mentioned earlier, the backend includes boards with Altera and Xilinx FPGAs. In developing the code for these devices we have used the libraries specific to each FPGA. These libraries use different naming conventions and programming styles, so we decided to entirely rewrite these modules in an abstract way, that are then mapped to the particular hardware by the synthesis tools. These components were mainly constituted by memories and MAC computing elements (multiply and accumulate). In this way we were able to render the code 100% portable to any FPGA, creating components that are completely independent of the system on which they are being implemented.

3.4 Modifications for the different board architecture

The DBBC hardware is markedly different from the Altera boards used in the original system. The input/output busses and the computer control logic are in particular completely different. We had thus to:

1) Create a new interface of the functional signal processing block with the outside system.
2) Modify the original code to interface it in the new hardware.

Sections 3.5 and 3.6 briefly illustrate these two steps.

3.5 DBBC interface

The system requires several input parameters: the bandwidth (<128 MHz), the center frequency (0 to 128 MHz), the integration time etc.
To set all these parameters, we have developed a general purpose module that receives generic commands from the outside (i.e., from the PC controlling the DBBC or remotely) and sets the appropriate registers in the FPGA boards. This is contained in a module *interface_dbbc,* described in [1], which can be used to set these parameters and to send the processed data to the control computer.
Everything outside the application specific signal processing part is described as a DBBC *skeleton block. This* is a VHDL file, in which are encapsulated all the platform signals, and where you can easily implement different kinds of projects. This is also described in [1].

3.6 Changes to the original code

The boards used in the original back-end have several FPGAs, programmed and optimized to process the signals, with a very complex data exchange system, because they were originally developed for different purposes. Our system is composed of a single, but larger, FPGA. The individual blocks described in fig. 4 have been thus modified to work in a single chip.

The old system described in fig.4 essentially consists of eight identical blocks which operate in parallel to analyze up to eight dual-polarization channels received from different feeds; the disposition of these logic blocks on different chips requires a complex data exchange mechanism between the boards and between the same chips. This data management and exchange system is handled by a single component included into each block.

Our single-chip implementation requires a simpler system. It is still possible, when necessary, to distribute operations among different chips by using the high-speed, multiple-channel, DBBC bus. In fig.5, we show the diagram of the new system:

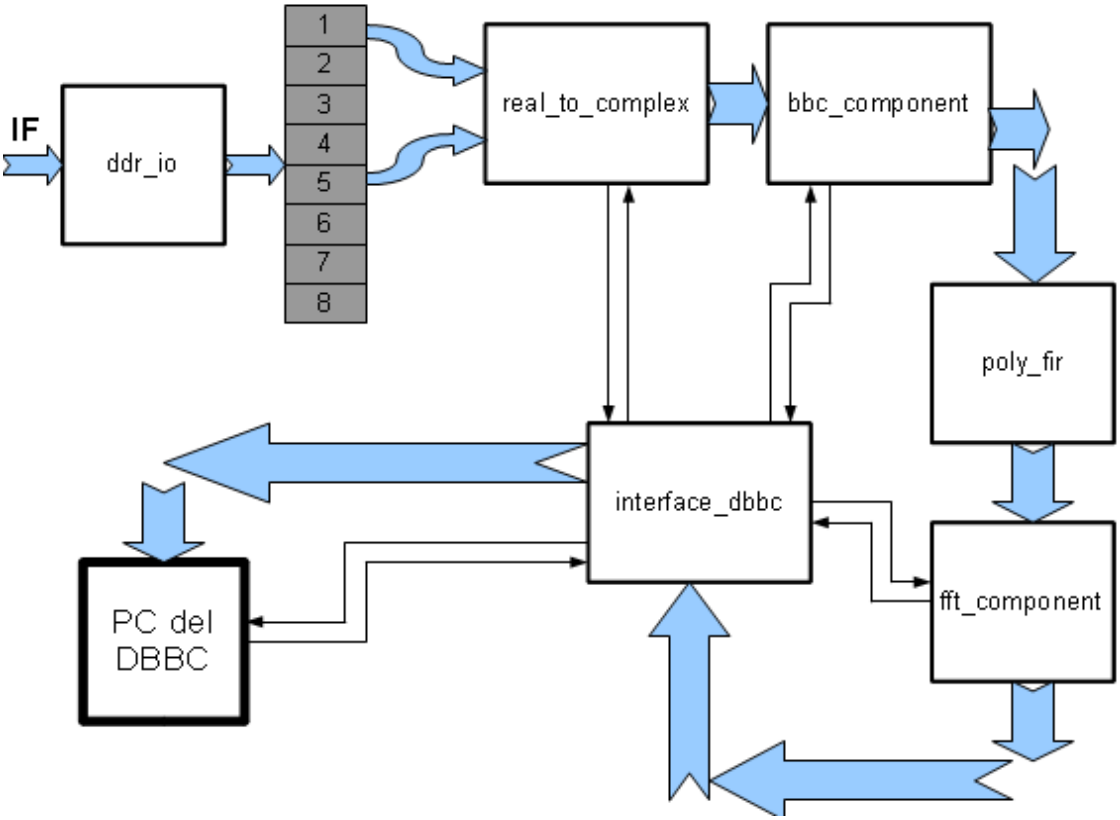

Figure 5: Block diagram after the porting

The diagram outlines the main blocks, indicated with their corresponding VHDL file names and the DBBC PC, indicated with bold lines.

The blue arrows indicate the signal in the processing pipeline, while the black arrows indicate bidirectional communication between the modules and the interface. The interface module allows to write into the registers of the modules and to monitor its internal signals, a very useful debug function.

The IF input signal, converted to digital form at 1.024 GHz, is first processed by the *ddr_io* block, which divides the samples acquired and provides eight parallel streams at 128 MHz.

The block *real_to_complex* receives two streams (1 and 5 in this case) and generates a signal having complex valued samples; that is sent to the *bbc_component* block, which selects the band and filter the signal.

After that the signal is processed by a polyphase filter (*poly_fir*), which provides the correct isolation between the spectral channels for the next block (*fft_component*). Due to resource limitation (especially on memory blocks) it was necessary to reduce the spectral resolution of the FFT block to 1024 spectral points.
The *interface_dbbc* block allow us to configure the system in real-time: we can change the band to analyze, the integration time etc; moreover it allows to visualize the processed signals on the DBBC PC.
Figure 5 represents a simplified system that manage a single input channel (single polarization). Due to limited FPGA resources, it is not possible to implement two bbc_component blocks in the same chip. The management of two channels, would require the duplication of the *real_to_complex* and of the *bbc_component* blocks, but not of the *poly_fir* and *fft_component* that can already process two streams at the same time. This requires the use of two CORE boards, with the FFT block on the second one.
The complete signal processing block (from signal conditioning to the FFT block) is available as a component, called *spectropolarimeter*, that can be instantiated as a whole inside the DBBC *skeleton*.

4 Conclusions and future projects

In this paper we described the porting of a spectropolarimeter (developed as a backend of a multi-feed receiver for the SRT) on the Digital Base Band Converter, a hardware platform being installed on all radiotelescopes of the EVN network.
The DBBC will be used as back-end for single dish observations when not used for VLBI observations, and this work provides a system usable for this observational modality, i.e. for single dish, single and double polarization observations with an instantaneous bandwidth of up to 128 MHz. SRT will be equipped with a DBBC provided with four elaboration boards and four data acquisition boards. This design, implemented in such a system, can analyze a bandwidth corresponding to 256 MHz (spectropolarimeter mode) or 512 MHz (spectrometer mode), covering most single dish requests.

We are developing new projects using both the skeleton framework described in [1] and variations on individual modules from this work. Implementing a polyphase filter bank, we can split the input bandwidth (4 Ghz single polarization or 2 Ghz dual-polarization) into smaller channels after the analog-to-digital conversion and choose to analyze one or more of these channels.

References

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